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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,458	09/26/2003	Takanori Ishikawa	01-506	7388

23400 7590 09/22/2005

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EXAMINER	
PATEL, DHARTI HARIDAS	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,458	ISHIKAWA ET AL.	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-14,16 and 17* is/are allowed.

6)☒ Claim(s) *1-4, 6-8* is/are rejected.

7)☒ Claim(s) *5,9,and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/26/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/26/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. **Claim Objections**

Claims 1 and 6-7 are objected to because of the following informalities: Claim 1 recites the limitation "the abnormal condition" in the second paragraph of the claim. There is insufficient antecedent basis for this limitation in the claim. The following is suggested wording for claims, which clarifies indefinite claim language.

Claim 1, line 9, "the abnormal condition" should read --- "an abnormal condition"

Claim 1, line 1, "circuit provided" should read --- "circuit is provided"

Claim 1, line 3, "to interrupts" should read --- "to interrupt"

Claim 6, line 4, and claim 7, line 4 both recite "of from". It is unclear what is meant by this claim language. For the purpose of applying art rejections, claims 6 and 7 are each interpreted to read "a current-carrying path from the input voltage."

Appropriate correction is required.

2. ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over LaVenture, Patent No. 4,034,232, in view of Gebara, Patent

No. 5,691,870. With respect to claim 1, LaVenture teaches a regulated power supply system 10, for a sensitive computer environment, which comprises a plurality of constant voltage generating circuits for changing an input voltage from an external electric power source A.C. INPUT to predetermined supply voltages to be supplied to a variety of loads, at least two of the constant voltage generating circuits having switching regulators 20a and 20b as disclosed in Col. 2, lines 56-59, lines 63-68, and Fig. 1. However, LaVenture does not disclose an abnormal condition detector circuit for detecting an occurrence of an abnormal condition in the constant voltage generating circuits in either one of the constant voltage generating circuits; and protection means provided for each of the constant voltage generating circuits to interrupt or limit an output of a supply voltage from the corresponding constant voltage generating circuits when the abnormal condition is detected.

Gebara teaches an abnormal condition detector circuit 102 for detecting an occurrence of an abnormal condition in a microprocessor 100 in a computer system C; and protection means provided for a microprocessor of the computer system to interrupt or limit an output of a supply voltage from the secondary voltage regulators when the abnormal condition is detected, wherein the abnormal condition detector circuit interrupts or limits the output of the supply voltage from the secondary voltage regulators to the microprocessor as disclosed in Col. 2, lines 38-60 and Fig. 1.

Both teachings are related by both being regulators for computer power supplies. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was mad to combine the teachings of Gebara, which teaches a circuit that monitors and disables power supply signals to a microprocessor in a computer system, into the regulated power supply system for a sensitive computer environment taught by LaVenture because the computer system requires all the voltages simultaneously in order to operate and interrupting the output from one regulator would effectively shut down the entire computer.

With respect to claim 2, Gebara teaches an abnormal condition detector circuit 102, wherein the protection means interrupts or limits the output of the supply voltage from the secondary voltage regulators, when the abnormal condition is detected by the abnormal condition detector circuit. This limitation is addressed by the connection of the abnormal condition detector in common to both of the switching regulator.

With respect to claim 3, Gebara teaches a circuit that monitors and disables power supply signals to a microprocessor in a computer system utilizing constant voltage generating circuits 101 includes a re-regulating circuit 102 for further changing the output from the power supply 101 as disclosed in Fig. 1; and the protection means including the re-regulating circuit, interrupts or limits the output from the re-regulating circuit when the abnormal condition is detected by the abnormal condition detecting circuit as disclosed in Col. 2, lines 38-44.

With respect to claims 6 and 7, it is well recognized to turn on or off any switching regulator that assumes a preset target voltage by turning on or off a transistor switch placed in the supply voltage side of the regulator. This is easily accomplished by interrupting the control signal to the transistor switch itself.

3. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over LaVenture, Patent No. 4,034,232, in view of Gebara, Patent No. 5,691,870 as applied to claims 1-3 and 6 above, and further in view of Brasfield, Patent No. 4,428,016. With respect to claim 4, LaVenture teaches a regulated power supply system 10, for a sensitive computer environment, which comprises a plurality of constant voltage generating circuits and Gebara teaches a circuit that monitors and disables power supply signals to a microprocessor in a computer system utilizing constant voltage generating circuit 101 having a re-regulating circuit 102 for further changing the output as disclosed in Fig. 1. However, both teachings do not disclose the constant voltage generating circuit having the re-regulating circuit includes over-current detector and an over-voltage detector.

Brasfield teaches an overload protected switching regulator for applying power to a load. The overload protected switching regulator comprises a current limit detector 27, which detects an electric current flowing through a current-carrying path and determines the current to be an over-current when it exceeds a preset threshold current value as disclosed in Col. 2, lines 42-50, and Fig. 3.; and an over-voltage detector 25 which detects a voltage input to the regulating circuit and determines the voltage to be an over-voltage when it exceeds a preset

threshold voltage value as disclosed in Col. 2, lines 33-36, and Fig. 3.; and wherein the protection means in all of the constant voltage generating circuits interrupts or limit the output from the switching regulator to interrupt or limit the output of the supply voltage, when the over-voltage or the over-current is detected as disclosed in Col. 17, lines 66-68, and Col. 18, lines 1-10.

All three teachings are related by being regulators. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Gebara, which teaches a circuit that monitors and disables power supply signals to a microprocessor in a computer system, and Brasfield, which teaches an overloaded protected switching regulator, into the regulated power supply system of LaVenture because such a modification would address other damaging fault types that are known to be problematic in power supplies.

With respect to claim 8, Brasfield teaches an overload protected switching regulator, which comprises an abnormal condition detector circuit that has at least one temperature detector means arranged close to a power switch to detect the over-heat of the transistor as disclosed in Col. 19, lines 8-15 and Fig. 7.

4. ***Allowable Subject Matter***

Claims 5, 9 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is an examiner's statement of reasons for indicating allowance: With respect to

claim 5, Gebara teaches a circuit for monitoring and disabling power supply signals to a microprocessor in a computer system utilizing a main power supply and secondary voltage regulators but does not teach the protection means having the re-regulating circuit interrupts or limits the output from the re-regulating circuit, when the over-voltage or the over-current is detected. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

With respect to claim 9, Brasfield teaches an abnormal condition detector circuit that has at least one temperature detector but does not disclose that each transistor and the temperature detector means are formed in a same semiconductor integrated circuit. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

With respect to claim 15, LaVenture teaches an electric power source device for supplying different electric power source voltage to the at least two circuits but does not teach a vehicle-mounted electronic control device having at least two circuits that receive different electric power source voltages from an external unit, and operate upon exchanging signals to each other. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

5. Claims 10-14 and 16-17 are allowed. The following is an examiner's statement of reasons for indicating allowance: LaVenture teaches a plurality of constant voltage generating circuits having respective switching regulators for

changing an input voltage from an external electric power source to predetermined supply voltages, but does not teach the attenuation means having such output voltage attenuation ratios that attenuated voltages assume the same value among the switching regulators possessed by all common constant reference voltage generating circuits, a reference voltage generating means and a reference waveform generating means that provides a reference waveform and is used in common by all of the common constant reference voltage generating circuits. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

4. **Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

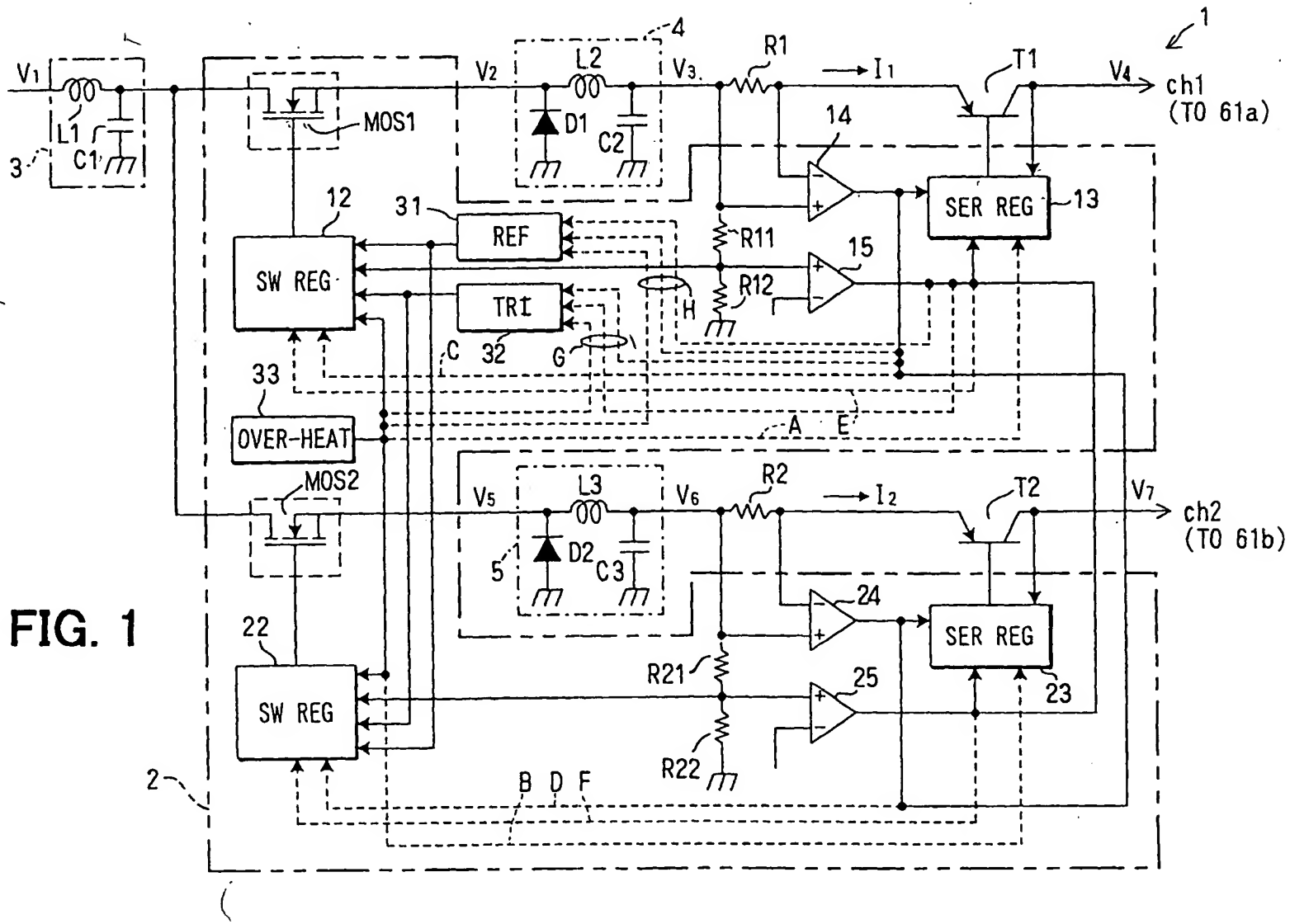
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-

direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DHP

Stephen W. Jackson
9-19-05

STEPHEN W. JACKSON
PRIMARY EXAMINER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C1
3
MOS1
V2
4
L2
D1
C2
V3
R1
I1
T1
V4
ch1
(TO 61a)
14
SER REG
13
12
31
REF
SW REG
R11
15
TRI
R12
H
C
32
G
33
OVER-HEAT
A
E
MOS2
V5
L3
D2
C3
5
V6
R2
I2
T2
V7
ch2
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23
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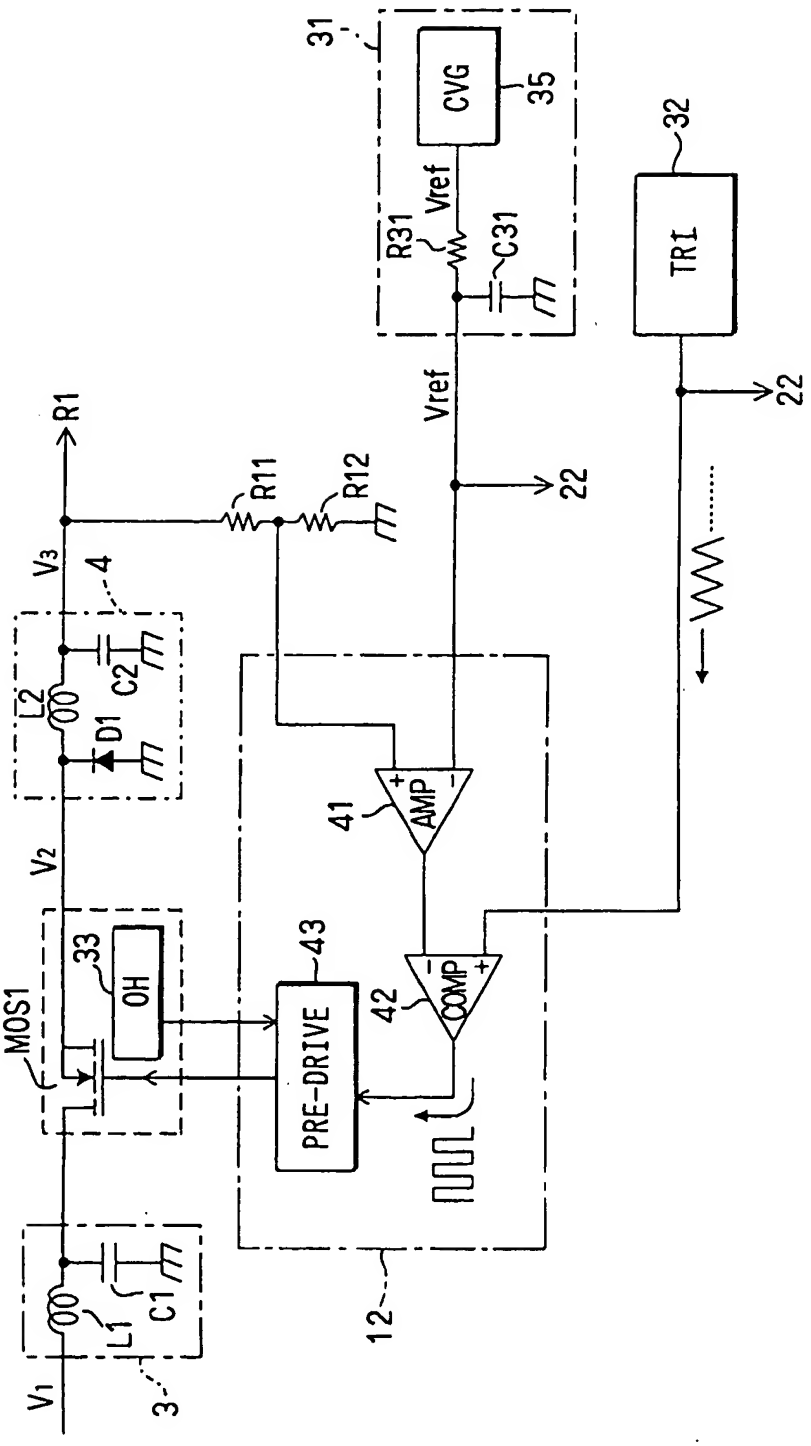
R22
2
B
D
F

FIG. 1

FIG. 2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R31
Vref
C31
R1
R11
R12
Vref
22
22
V3
4
L2
C2
D1
41
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V2
33
OH
MOS1
43
PRE-DRIVE
42
COMP
12
L1
C1
V1
3

FIG. 3

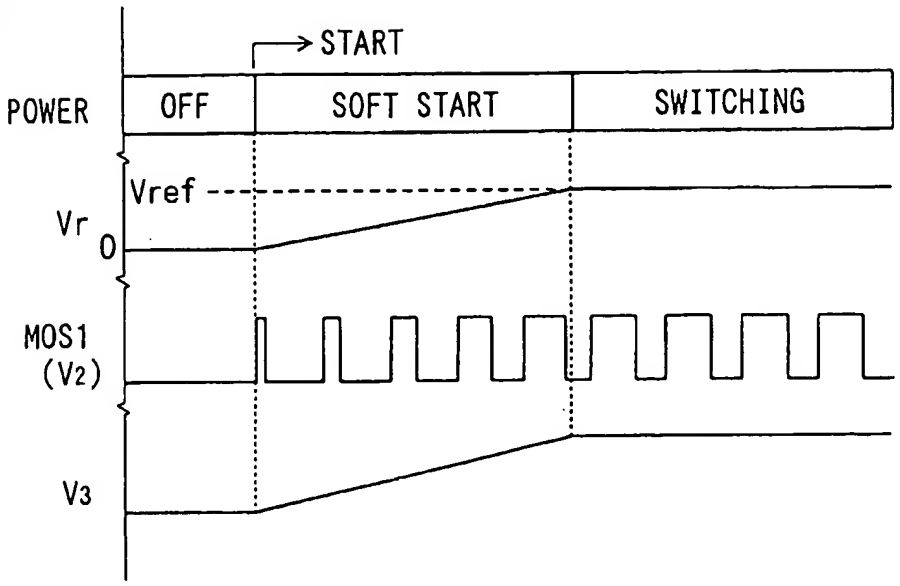


FIG. 5A

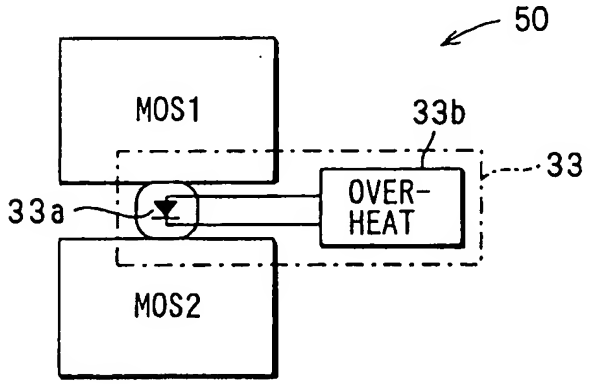


FIG. 5B

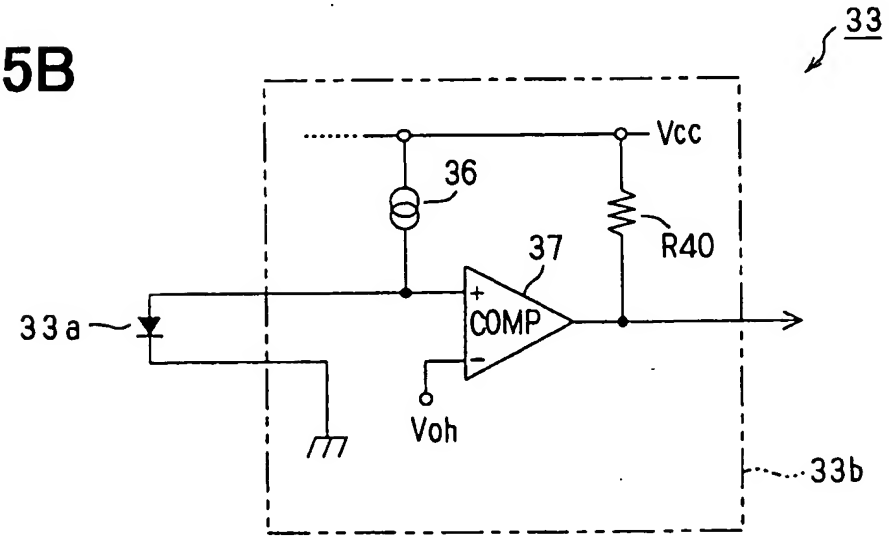


FIG. 4

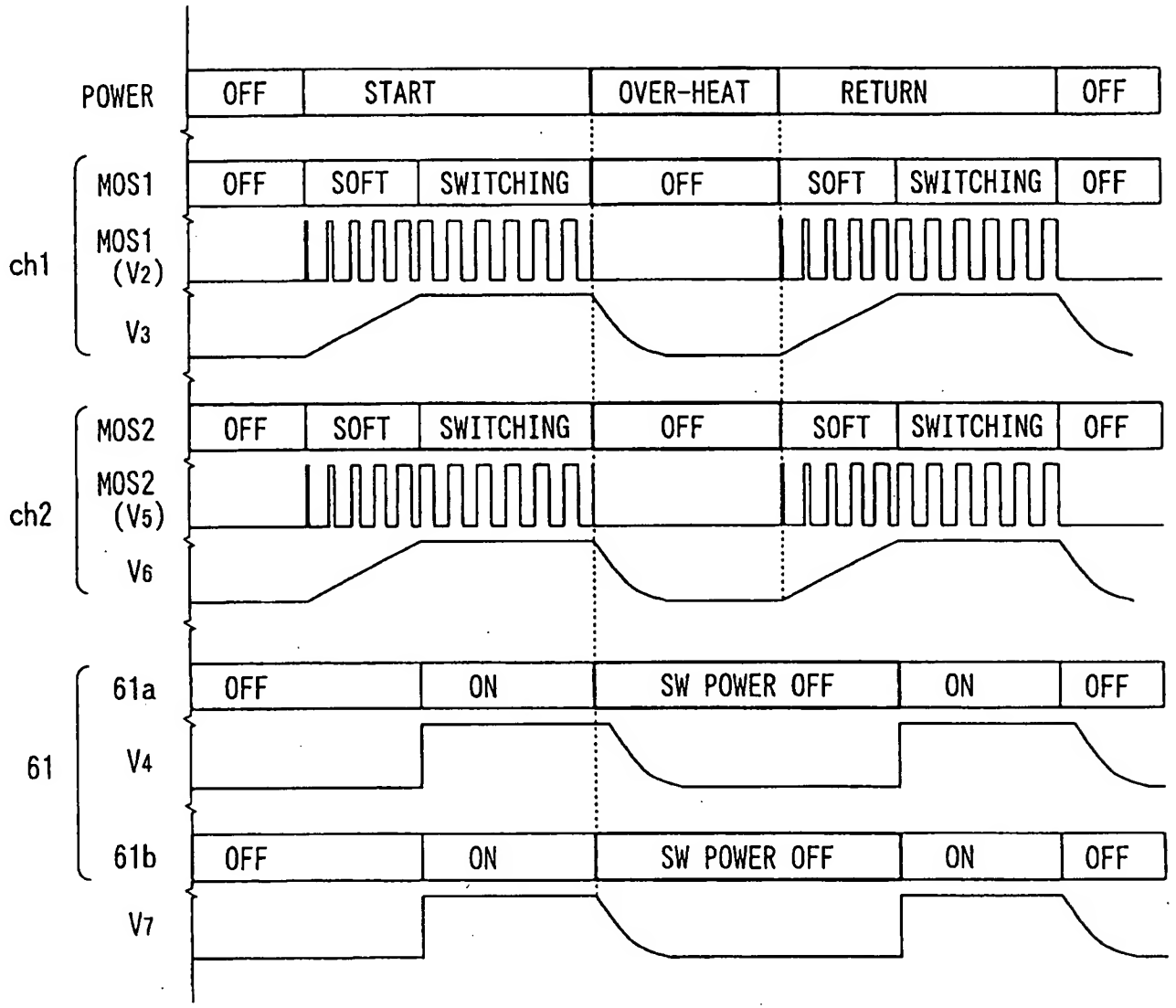
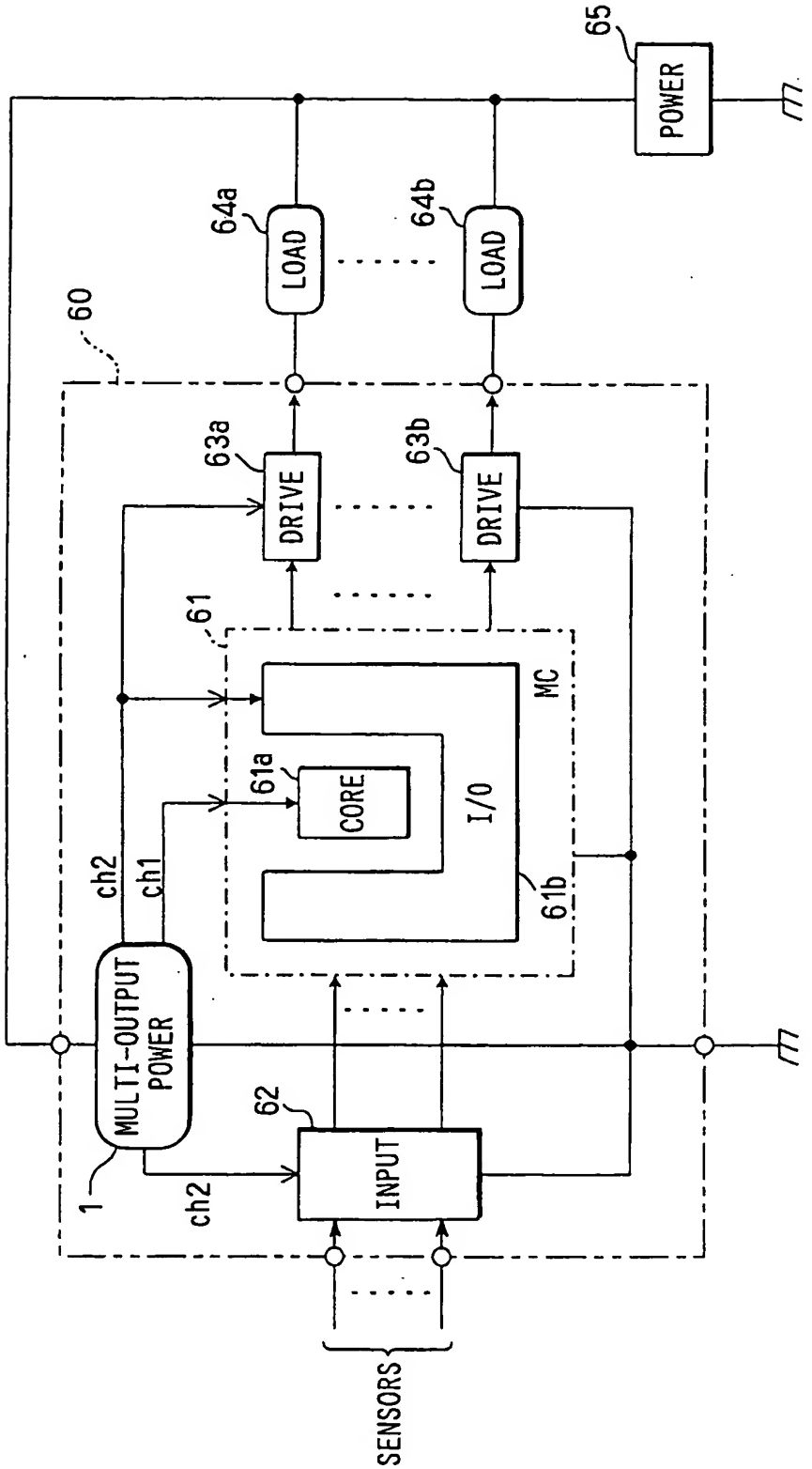

POWER
OFF
START
OVER-HEAT
RETURN
OFF
MOS1
OFF
SOFT
SWITCHING
OFF
SOFT
SWITCHING
OFF
ch1
MOS1
(V2)
V3
MOS2
OFF
SOFT
SWITCHING
OFF
SOFT
SWITCHING
OFF
ch2
MOS2
(V5)
V6
61a
OFF
ON
SW POWER OFF
ON
OFF
61
V4
61b
OFF
ON
SW POWER OFF
ON
OFF
V7

FIG. 6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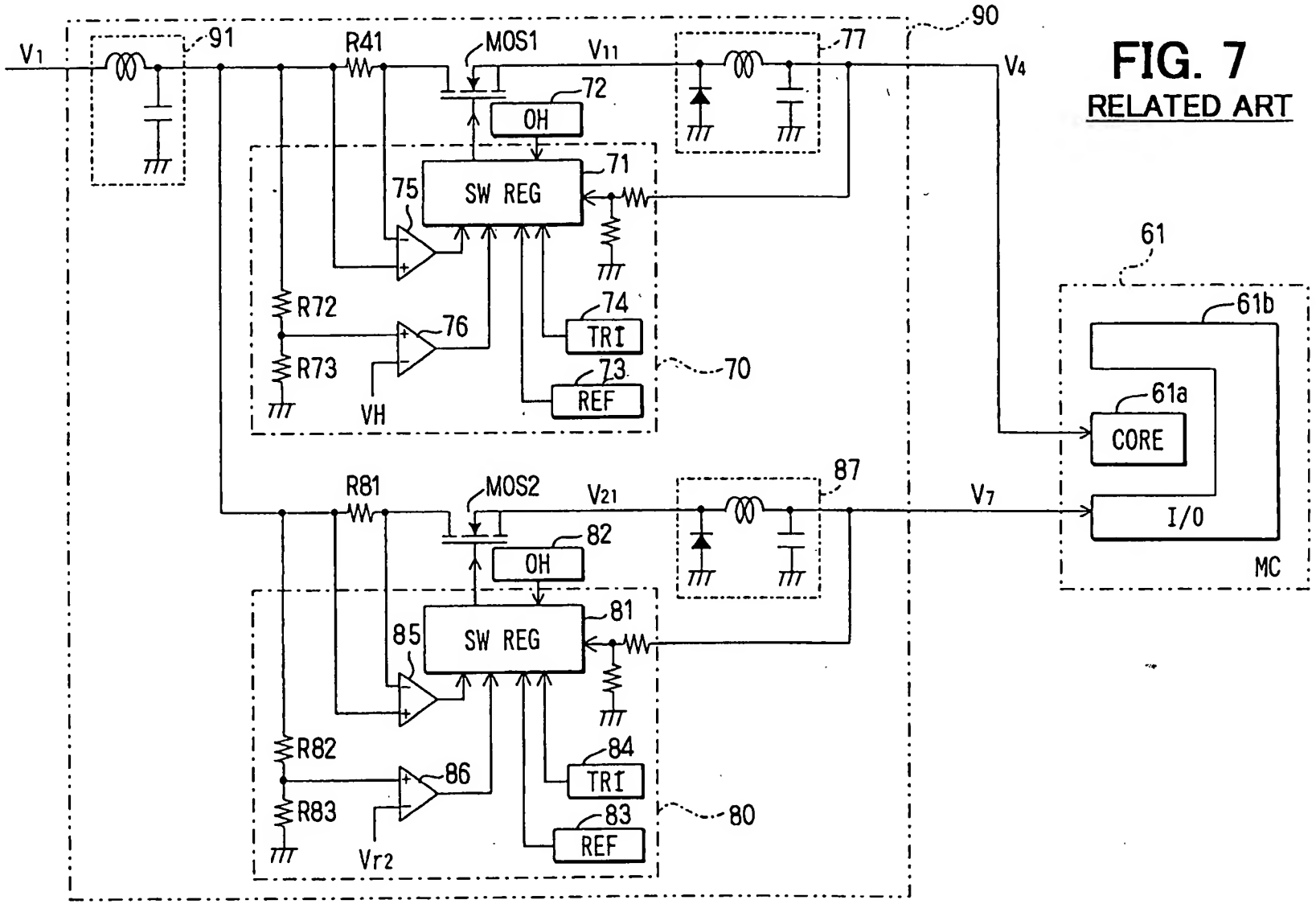

FIG. 7
RELATED ART

FIG. 8
RELATED ART